CLAIMS

1. A semiconductor device comprising:

a single crystal substrate formed of a substrate material;

a dielectric layer overlying the single crystal substrate, the dielectric layer having at least one opening which has a first portion and an overlying second portion, the first portion having a predetermined depth and a predetermined width, wherein a ratio of the predetermined depth to the predetermined width is greater than one;

a first material having a first portion and a second portion, the first portion of the first material filling the first portion of the at least one opening, defects for relaxing strain at an interface between the first material and the substrate material existing only within the first portion of the first material due to the ratio being greater than one; and

the second portion of the first material and an overlying second material different than the first material filling the overlying second portion of the at least one opening, the second material having a thickness which is less than a critical thickness to maintain the second material in a strained state, the second portion of the first material being substantially defect free, the second material functioning as a channel for charge carriers.

2. The semiconductor device of claim 1 wherein part of the second portion of the first material is laterally extended beyond the at least one opening to form a T-shape structure.

3. The semiconductor device of claim 2 further comprising:

a control electrode formed overlying a predetermined portion of the second material;

a first current electrode formed in the second material and offset from a first side of the control electrode; and

a second current electrode formed in the second material and offset from a second side of the control electrode.

4. The semiconductor device of claim 3 wherein the first current electrode is formed in both the second material and a third portion of the first material, and the second current electrode is formed in both the second material and a fourth portion of the first material.

5. The semiconductor device of claim 3 wherein the control electrode is aligned vertically overlying the at least one opening thereby reducing floating body effects.

6. The semiconductor device of claim 3 further comprising:

a second dielectric layer overlying the dielectric layer, the second dielectric layer being a different dielectric material than the first dielectric layer and being adjacent the first current electrode and the second current electrode.

7. The semiconductor device of claim 3 further comprising:

a second opening in the dielectric layer that is filled with the first material and the overlying second material, the second opening having an overlying second control electrode adjoined by a third current electrode and a fourth current electrode, the third current electrode being in direct physical contact with the second current electrode via a lateral extension of part of the second portion of the first material.

8. The semiconductor device of claim 3 further comprising:

a second opening in the dielectric layer that is filled with the first material and the overlying second material, the second opening having an overlying second control electrode adjoined by a third current electrode and a fourth current electrode, the first current electrode and the second current electrode being electrically isolated from the third current electrode and the fourth current electrode by the dielectric layer.

9. A semiconductor device comprising:

a single crystal substrate;

an overlying dielectric layer having a first opening and a second opening with an overlying third opening that encompasses both the first opening and the second opening;

a single crystal material filling the first opening, the second opening and a portion of the third opening, the single crystal material having controlled defects for relaxing strain at an interface between the single crystal material and the substrate material existing only at interfaces in the first opening and the second

opening, the single crystal material overlying controlled defect areas being substantially defect free;

a single crystal strain material overlying the single crystal material and filling a remaining portion of the third opening, a thickness of the single crystal strain material being small enough to substantially avoid defect formation;

a first transistor formed overlying and within at least the single crystal strain material and aligned to the first opening, the first transistor having a control electrode and first and second current electrodes; and

a second transistor formed overlying and within at least the single crystal strain material and aligned to the second opening, the second transistor having a control electrode and first and second current electrodes, the first current electrode of the first transistor being in direct physical contact with the second current electrode of the second transistor allowing electrical interoperability between the first transistor and second transistor.

10. The semiconductor device of claim 9 wherein the overlying dielectric layer further comprises:

a first dielectric overlying the substrate that defines the first opening and the second opening; and

a second dielectric that is a different material from the first dielectric that defines the third opening, the different material being used to avoid excessive etching of the first dielectric and second dielectric when making electrical contact to either the first current electrode or the second current electrode.

11. A method of forming an isolation structure in a semiconductor, comprising:

providing a single crystal substrate;

forming a first dielectric overlying the substrate;

forming a second dielectric overlying the first dielectric, the second dielectric being a different material than the first dielectric;

forming a first opening having a first diameter completely through the first dielectric and forming a second opening having a second diameter completely through the second dielectric, the second diameter being equal to or greater than the first diameter wherein the first opening and the second opening expose a surface of the single crystal substrate;

filling the first opening and a portion of the second opening with a first single crystal semiconductor material having a relaxed state by having defects for a controlled depth from the single crystal substrate to a predetermined height, a remainder of the first single crystal semiconductor material not having defects;

filling a remaining portion of the second opening with a second single crystal semiconductor material that is strained by having a predetermined thickness that does not exceed a critical thickness where defects begin to form; and

forming a transistor overlying and within at least a portion of the second opening.

12. The method of claim 11 further comprising:

forming the first opening to having a predetermined width and a predetermined depth, a ratio of the predetermined depth to the predetermined width being greater than one in order to define the controlled depth of defects of the first single crystal semiconductor material.

13. The method of claim 11 further comprising:

using the different material of the second dielectric from the first dielectric as a control parameter to avoid excessive etching of the first dielectric and second dielectric when making electrical contact to a current electrode of the transistor.

14. The method of claim 11 further comprising:

forming a third opening having a third diameter completely through the first dielectric and forming a fourth opening having a fourth diameter completely through the second dielectric, the fourth diameter being equal to or greater than the third diameter wherein the third opening and the fourth opening expose the surface of the single crystal substrate; and

filling the third opening and a portion of the fourth opening with the first single crystal semiconductor material having the relaxed state by having defects for a controlled depth from the single crystal substrate to the predetermined height, the remainder of the first single crystal semiconductor material not having defects;

filling a remaining portion of the fourth opening with the second single crystal semiconductor material that is strained by having a predetermined thickness that does not exceed a critical thickness where defects begin to form; and

forming a second transistor overlying and within at least a portion of the fourth opening, the second transistor being laterally adjacent the first transistor and having a current electrode directly touching a current electrode of the first transistor.

15. The method of claim 11 further comprising:

forming a third opening having a third diameter completely through the first dielectric and forming a fourth opening having a fourth diameter completely through the second dielectric, the fourth diameter being equal to or greater than the third diameter wherein the third opening and the fourth opening expose the surface of the single crystal substrate; and

filling the third opening and a portion of the fourth opening with the first single crystal semiconductor material having the relaxed state by having defects for a controlled depth from the single crystal substrate to the predetermined height, the remainder of the first single crystal semiconductor material not having defects;

filling a remaining portion of the fourth opening with a fourth single crystal semiconductor material that is strained by having a predetermined thickness that does not exceed a critical thickness where defects begin to form; and

forming a second transistor overlying and within at least a portion of the fourth opening, the second transistor being laterally adjacent the first transistor but not directly electrically connected to the first transistor.

16. A method of forming an isolation structure in a semiconductor, comprising:

providing a single crystal substrate;

forming a dielectric overlying the single crystal substrate;

forming a first opening having a first diameter through a portion of the dielectric and forming a second opening having a second diameter through a remainder of the dielectric, the second diameter being equal to or greater than the first diameter wherein the first opening and the second opening expose a surface of the single crystal substrate;

filling the first opening and a portion of the second opening with a first single crystal semiconductor material having a relaxed state by having defects for a controlled

depth from the single crystal substrate to a predetermined height, a remainder of the first single crystal semiconductor material not having defects;

filling a remaining portion of the second opening with a second single crystal semiconductor material that is strained by having a predetermined thickness that does not exceed a critical thickness where defects begin to form; and

forming a transistor overlying and within at least a portion of the second opening.

17. The method of claim 16 further comprising:

forming the first opening to having a predetermined width and a predetermined depth, a ratio of the predetermined depth to the predetermined width being greater than one in order to define the controlled depth of defects of the first single crystal semiconductor material.

18. The method of claim 16 further comprising:

forming a third opening having a third diameter through a second portion of the dielectric and forming a fourth opening having a fourth diameter through a remainder of the second portion of the dielectric, the fourth diameter being equal to or greater than the third diameter wherein the third opening and the fourth opening expose the surface of the substrate;

filling the third opening and a portion of the fourth opening with the first single crystal semiconductor material having the relaxed state by having defects for a controlled depth from the single crystal substrate to the predetermined height, the remainder of the first single crystal semiconductor material not having defects;

filling a remaining portion of the fourth opening with the second single crystal semiconductor material that is strained by having a predetermined thickness that does not exceed a critical thickness where defects begin to form; and

forming a second transistor overlying and within at least a portion of the fourth opening, the second transistor being laterally adjacent the first transistor and having a current electrode directly touching a current electrode of the first transistor.

19. The method of claim 16 further comprising:

forming a third opening having a third diameter through a second portion of the dielectric and forming a fourth opening having a fourth diameter through a remainder of the second portion of the dielectric, the fourth diameter being equal to or greater than the third diameter wherein the third opening and the fourth opening expose the surface of the substrate;

filling the third opening and a portion of the fourth opening with the first single crystal semiconductor material having the relaxed state by having defects for a controlled depth from the single crystal substrate to the predetermined height, the remainder of the first single crystal semiconductor material not having defects;

filling a remaining portion of the fourth opening with the second single crystal semiconductor material that is strained by having a predetermined thickness that does not exceed a critical thickness where defects begin to form; and

forming a second transistor overlying and within at least a portion of the fourth opening, the second transistor being laterally adjacent the first transistor but not directly electrically connected to the first transistor.

20. The method of claim 16 further comprising:

forming the first single crystal material with silicon germanium;

forming the second single crystal material with silicon;

forming the single crystal substrate with silicon; and

forming the dielectric with one of silicon dioxide or silicon nitride.